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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,942	04/15/2004	Mitsuhiko Otani	10873.1453US01	7557

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EXAMINER	
KARIMY, MOHAMMAD TIMOR	
ART UNIT	PAPER NUMBER
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/824,942	OTANI, MITSUHIKO	
	Examiner	Art Unit	
	Mohammad Timor Karimy	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishikura et al. (US Pub 2002/0079556 A1).

Ishikura discloses in figure 5B, a semiconductor integrated circuit device, comprising a digital circuit 51 and an analog circuit 50 that are disposed on a surface of a semiconductor substrate 52.

Ishikura further teaches a dummy layer 13a made of polysilicon that is the same as polysilicon composing a gate of a transistor is disposed between the digital circuit 51 and the analog circuit 50. Ishikura explicitly teaches in paragraphs [16-17] that P-type region 52 has increased resistance due to analog and digital regions being sufficiently spaced away from one another (note that region 52 is under the dummy gate layers 13a).

With respect to claim 2, Ishikura discloses the semiconductor integrated circuit device according to claim 1, wherein a dummy diffused region 11a is further provided between the dummy layer part and one of the digital circuit part 51 and the analog circuit part 50.

Ishikura further discloses in paragraph 0082 a floating node with no fixed potential level in the dummy region, which could perform as the power-supply potential.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art admitted by Hasegawa (US Patent 5,900,927) in view of Ishikura et al. (US pub 2002/0079556 A1).

With regard to claim 3, the admitted prior art teaches in column 1 lines 31-66 and column 2 lines 1-4, a digital circuit for driving a sensor 205 and an analog circuit for processing an image detecting signal that is outputted from the sensor (see figures 34A and 34B). However, the admitted prior art by Hasegawa does not teach dummy polysilicon region between the digital and analog circuits. Nonetheless, Ishikura teaches a dummy region including a dummy polysilicon gate 13a and dummy diffused region 11a between a digital 51 and analog 50 circuits. The prior art admitted by Hasegawa and Ishikura are analogous art - both deal with analog and digital circuits of image sensor devices. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to form a dummy region between the digital and analog

circuits as taught by Ishikura in order to suppress noise propagation. The motivation for doing so would have been to reduce noise. Therefore, it would have been obvious to combine the admitted prior art by Hasegawa and Ishikura for the benefit of suppressing noise propagation.

With respect to claim 5, the recitation "camera" in line 1 has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

With respect to the additional limitations of claim 5, the prior art admitted by Hasegawa teaches in column 1 lines 31-66 and column 2 lines 1-4, a semiconductor integrated circuit device comprising a digital circuit for driving an imaging element 205 and an analog circuit for processing an image detecting signal that is outputted from the imaging element 205 (see figures 34A and 34B). However, the prior art does not teach a dummy polysilicon region between the digital and analog circuits. Nonetheless, Ishikura teaches a dummy region including a dummy polysilicon gate 13a and dummy diffused region 11a between a digital 51 and analog 50 circuits. The admitted prior art by Hasegawa and Ishikura are analogous art, namely both deal with analog and digital circuits of image sensor devices. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to form a dummy region between the

digital and analog circuits as taught by Ishikura in order to suppress noise propagation. The motivation for doing so would have been to reduce noise. Therefore, it would have been obvious to combine Hasegawa's admitted prior art and Ishikura for the benefit of suppressing noise propagation.

5. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa's admitted prior art in view of Hasegawa (US Patent 5,900,927).

With respect to claim 4, Hasegawa's admitted prior art teaches a sensor device with the accordance to the conventional art as described in rejection for claim 3. However, the prior art does not explicitly teach the sensor being a CCD (Charge Coupled Device). Nonetheless, Hasegawa teaches in column 9 lines 54-67 and column 10 lines 1-4 a CCD being part of a path finder, where it transfers the generated electric charges. The prior art and Hasegawa are from the same field of endeavor, namely digital and analog circuits and sensors. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a CCD as taught by Hasegawa in the prior art's sensor device for the purpose of transferring electric charges. The motivation for doing so would have been the transfer of generated electric charges. Therefore, it would have been obvious to combine the admitted prior art with Hasegawa to obtain a charge transfer mechanism.

Response to Arguments

6. Applicant's arguments filed 01/10/2007 have been fully considered but they are not persuasive.

With respect to claim 1, applicant argues that the dummy layer is disposed directly on a portion of semiconductor substrate that is of higher resistance. The prior art, Ishikura, explicitly teaches a dummy gate 13a disposed on a region 52 of the substrate, wherein the P-type substrate 52 has an increased resistance due to the sufficient space between the analog and digital circuits (paragraphs [16-17]).

With respect to claim 2, Ishikura explicitly teaches in figure 5B dummy diffused regions between a dummy layer part and one of the analog circuit part and a digital circuit part.

In light of the above, applicant's argument is not persuasive.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad Timor Karimy whose telephone number is 571-272-9006. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mtk

EUGENE LEE
PRIMARY EXAMINER